

AMENDMENT AND RESPONSE

PAGE 2

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

IN THE CLAIMS

1. (Previously presented) An integrated circuit for monitoring and controlling multiple power outputs from a power supply that generates a first primary power voltage and one of more secondary primary power voltages, comprising:

an input means for receiving the first primary and secondary primary power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level;

means for delaying connection of the first primary and secondary primary power voltages to the controlled voltage power outputs for a selected delay time after the first primary power voltage reaches the reference threshold level; and

means for initiating a soft start after the selected delay time has expired.

2. (Original) The integrated circuit of claim 1 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

3. (Previously presented) The integrated circuit of claim 1 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

4. (Original) The integrated circuit of claim 3 wherein the delaying means comprises a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the input power supply voltages to the controlled outputs for the selected delay time.

AMENDMENT AND RESPONSE

PAGE 3

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

5. (Original) The integrated circuit of claim 1 further comprising a linear controller for controlling the output voltage of each of the power output voltages of the power monitor circuit.

6. (Previously presented) A computer system with monitored power comprising in combination:

a power supply for generating a first primary dc power voltage and one or more secondary primary dc power voltages, a motherboard comprising multiple units including a memory unit and a central processing unit, wherein said units may require different operating voltages; and a power monitoring integrated circuit disposed between the power supply and the motherboard for controlling supply power from the power supply to the mother board, said power monitoring circuit comprising,

input means for receiving the first primary and secondary primary power voltages from the power supply;

means for controlling the received power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the controlled power output voltages to the computer for a selected delay time after the first primary power voltage reaches the reference threshold level, wherein the selected time delay insures the power output voltages are stabilized.

7. (Previously presented) The computer system of claim 6 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a usable and effective voltage level.

8. (Previously presented) The computer system of claim 6 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

AMENDMENT AND RESPONSE

PAGE 4

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

9. (Original) The computer system of claim 8 wherein the delaying means comprised a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the controlled power output voltages to the computer for the selected delay time.

10. (Original) The computer system of claim 6 wherein the means for controlling the output voltages comprises a plurality of linear controllers with each linear controller controlling the output voltage of one of the power output voltages of the power monitor circuit.

11. (Previously presented) A method for monitoring and controlling power from a power supply that generates a first primary power voltage and one or more secondary primary power voltages related to the first primary power voltage, comprising:

- receiving the first and secondary primary power voltages from the power supply;
- controlling the received power voltages to generate controlled voltage power outputs;
- comparing a signal representative of the first primary power voltage to a reference signal;
- sensing when the first primary power output voltage reaches or exceeds a threshold

reference level; and

- delaying connection of the power supply controlled voltage power outputs for a selected delay time after the first primary power output voltage reaches the reference threshold level.

12. (Previously presented) The method of claim 11 further comprising, generating an output signal indicating that the first primary power voltage has reached at least 90% of its target value.

13. (Previously presented) The method of claims 11, wherein the step of comparing a signal representative of the first primary power voltage to a reference voltage further comprises:

- dividing a signal representative of the first primary power voltage and comparing the voltage divided signal to a threshold reference voltage.

14. (Previously presented) The method of claim 13 wherein the delaying step comprises timing an interval starting when the voltage divided signal exceeds the threshold reference signal and

AMENDMENT AND RESPONSE

PAGE 5

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

delaying connection of the controlled voltage power outputs to the computer for a selected delay time.

15. (Original) The method of claims 11 further comprising linearly controlling each of the power output voltages of the power monitor circuit.

16. (Previously presented) A power monitor circuit comprising:
a first input adapted to receive a first primary voltage from a power supply;
one or more secondary inputs to receive one or more secondary primary voltages from the power supply, wherein the one or more secondary primary voltages are related to the first primary voltage;
a comparator circuit adapted to compare the first primary voltage with a reference voltage; and
a time delay circuit adapted to delay an output of the one or more secondary primary voltages by a select period of time once the first primary voltage equals or exceeds the reference voltage.

17. (Previously presented) The power monitor circuit of claim 16, wherein the comparator circuit further comprises:
a resistor divider network adapted to divide the first primary voltage, the resistor divider network comprising:
a first resistor of a first select value, and
a second resistor of a second select value, the first and second resistor being adapted to divide the first primary voltage into a select first divided primary voltage; and
a comparator having a first input coupled to the resistor divider network to receive the select divided first primary voltage, the comparator having a second input coupled to receive the reference voltage, the comparator further having an output coupled to the time delay circuit.

18. (Previously presented) The power monitor circuit of claim 16, wherein the reference voltage is approximately equal to 90% of the first primary voltage.

AMENDMENT AND RESPONSE

PAGE 6

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

19. (Previously presented) The power monitor circuit of claim 16, wherein the time delay circuit outputs the first primary and one or more secondary primary voltages approximately 40ms after the primary voltage equals or exceeds the reference voltage.

20. (Previously presented) The power monitor circuit of claim 16, wherein the first primary voltage is approximately equal to 12 volts, one of the secondary primary voltages is approximately equal to 3.3 volts and another of the secondary primary voltages is approximately equal to 5 volts.

21. (Previously presented) A power monitor circuit for monitoring a voltages from a power supply wherein the power supply derives two or more associated voltages, the power monitor circuit comprising:

- a first input adapted to receive one voltage of the two or more voltages from the power supply;

- a secondary input for each of the remaining two or more voltages, each secondary input adapted to receive an associated one of the remaining two or more voltages;

- an output for each of the two or more voltages;

- a comparator circuit adapted to compare the one voltage received at the first input with a reference voltage; and

- a time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a select period of time after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage.

22. (Previously presented) The power monitor circuit of claim 21, wherein the one voltage received on the first input is a first primary voltage and the remaining two or more voltages are secondary primary voltages.

23. (Previously presented) The power monitor circuit of claim 21, wherein the reference voltage is in relation to 90% of the nominal setting of the one voltage received at the first input.

AMENDMENT AND RESPONSE

PAGE 7

Serial No.: 09/552,117

Filing Date: April 19, 2002

Attorney Docket No. 125.037US01

Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

24. (Previously presented) The power monitor circuit of claim 21, wherein the select period of time is approximately 40ms.

25. (Previously presented) The power monitor circuit of claim 21, further comprising:
a voltage divider adapted to divide the one voltage received on the first input, wherein the divided one voltage received on the first input is compared to the reference voltage.